IN THE CLAIMS:

The text of all pending claims, (including withdrawn claims) is set forth below. Cancelled and not entered claims are indicated with claim number and status only. The claims as listed below show added text with underlining and deleted text with ~~strikethrough~~. The status of each claim is indicated with one of (original), (currently amended), (cancelled), (withdrawn), (new), (previously presented), or (not entered).

Please AMEND claims 1, 2, 5, 7, and 10, and cancel claim 9 without prejudice or disclaimer of the subject matter contained therein in accordance with the following:

1. (CURRENTLY AMENDED) An organic EL display control system comprising:

a display panel including data lines and scan lines, the data lines arranged in a transverse direction, the scan lines arranged in a perpendicular direction to the data lines; and

a driver controller having a display RAM storing data;~~,~~

wherein the data is vertically written on and vertically read from the display RAM, and the read data is transmitted to the display panel.

2. (CURRENTLY AMENDED) The system of claim 1, wherein the driver controller further comprises:

a common driver circuit connected to the scan lines of the display panel;

a segment driver circuit connected to the data lines of the display panel,

a page address generating circuit connected to the display RAM through address buses and designating vertically a page address to store the data during a write operation;

a data latch circuit connected to the display RAM through data buses so that the data of a column ~~may be~~is output from the display RAM at a time during a read operation;

a line address generating circuit connected to the display RAM through address buses and designating the column to be displayed during a read operation;

a column address generating circuit connected to the display RAM through address buses and designating a column address during a write operation; and

a controller controlling each of the common driver circuit, the segment driver circuit, the page address generating circuit, the data latch circuit, the line address generating circuit, and the column address generating circuit.

3. (ORIGINAL) The system of claim 1, wherein a line length between the common driver circuit and the scan lines is shorter than that between the segment driver circuit and the data lines.

4. (ORIGINAL) The system of claim 1, wherein the data is an image, and the image is turned up by conversely changing a connection order of pins of an input side of the display RAM.

5. (CURRENTLY AMENDED) The system of claim 1, wherein the data is an image, and the image is turned up by conversely changing a connection order of pins of an ~~input~~output side of the display RAM.

6. (ORIGINAL) The system of claim 2, wherein a line length between the common driver circuit and the scan lines is shorter than that between the segment driver circuit and the data lines.

7. (CURRENTLY AMENDED) An organic EL display control system, comprising:

a display panel including a segment terminal and a common terminal, the segment terminal connected to data lines, the common terminal connected to scan lines arranged in a perpendicular direction to the data lines; and

a driver controller having a display RAM storing data and outputting the data from the display RAM in the same direction as a longitudinal direction of the scan lines;

wherein a line length between the common terminal and the driver controller is shorter than that between the segment terminal and the driver controller.

8. (ORIGINAL) The system of claim 7, wherein the data lines are arranged in a transverse direction, and the scan lines are arranged in a vertical direction.

9. (CANCELLED)

10. (CURRENTLY AMENDED) The system of claim 7, wherein the driver controller comprises:

a common driver circuit connected to the common terminal of the display panel;

a segment driver circuit connected to the segment terminal of the display panel;

a page address generating circuit connected to the display RAM through address buses and designating vertically a page address to store the data during a write operation;

a data latch circuit connected to the display RAM through data buses so that the data of a column ~~maybe~~is output from the display RAM at a time during a read operation;

a line address generating circuit connected to the display RAM through address buses and designating the column to be displayed during a read operation;

a column address generating circuit connected to the display RAM through address buses and designating a column address during a write operation; and

a controller controlling each of the common driver circuit, the segment driver circuit, the page address generating circuit, the data latch circuit, the line address generating circuit, and the column address generating circuit.

11. (ORIGINAL) The system of claim 7, wherein the data is an image, and the image is turned up by conversely changing a connection order of pins of an output side of the display RAM.

12. (ORIGINAL) The system of claim 10, wherein a line length between the common driver circuit and the common terminal is shorter than that between the segment driver circuit and the segment terminal.